Amirkabir University of Technology
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Computer Engineering and Information Technology Department

PhD Dissertation

Proposing a Framework for Designing Scalable and Fault-Toletant Quantum Computers

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October 2018

Abstract

One of the most important challenges in realizing large-scale, fault-tolerant quantum computers is that quantum systems are highly susceptible to noise caused by decoherence and imperfect quantum operations. Using quantum error correction codes and fault-tolerant operations are the common approaches to address this problem. However, these approaches generally incur a significant resource overhead for the implementation of a quantum computer and limit its scalability.

In this research, a framework comprising of two parts, namely the underlying platform and the physical design flow, is proposed. Technology, error correction code, architecture and computational model are the main elements of the underlying platform. In this research, ion-trap has been selected as the fabrication technology. Then, three implementations of quantum error correction codes that reduce the overhead of applying non-transversal gates in a fault-tolerant manner are proposed. In comparison with the common approach of magic state distillation, the proposed approaches reduce the overhead of applying non-transversal gates by 85% on average. Subsequently, an architecture that removes long distance communications in computational units by uniform distribution of logical qubits in computational units and eliminates the need for algorithmic placement and routing in our physical design flow is introduced.

The physical design flow that is suggested in this dissertation consists of a low-level and a high-level mapper. The low-level mapper computes the cost metrics of the logical operations and stores them in a database. The high-level mapper maps an input circuit on the platform based on the stored cost metrics. Partitioning, error analysis and scheduling are the main parts of the high-level mapper. The proposed partitioning algorithm reduces the number of photonic interconnections by 45% on average. Simulation results show that the delay of benchmark circuits is reduced 17 times.

Key Words: Quantum computation, Scalable quantum computer, Fault-tolerant quantum computer, Quantum error correction code, Physical design.