Parallel Hardware Implementation of Cellular Learning Automata Based Evolutionary Computing (CLA-EC) on FPGA

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ABSTRACT

The CLA-EC is a model obtained by combining the concepts of cellular learning automata and evolutionary algorithms. The parallel structure of the CLA-EC makes it suitable for hardware-based applications including evolvable hardware. In this paper, based on the SIMD model, a parallel architecture is proposed and implemented on FPGA. Simulation results show that the proposed architecture can solve optimization problems thousands times faster than the sequential implementations.

INDEX TERMS

Primary Classification:
F. Theory of Computation
F.1 COMPUTATION BY ABSTRACT DEVICES
F.1.1 Models of Computation
Subjects: Unbounded-action devices (e.g., cellular automata, circuits, networks of machines)

Additional Classification:
B. Hardware
B.6 LOGIC DESIGN
B.6.1 Design Styles
Subjects: Cellular arrays and automata

B.7 INTEGRATED CIRCUITS

B.7.1 Types and Design Styles

Subjects: Gate arrays

General Terms:
Algorithms, Design, Theory

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