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High-level Energy Estimation of Template-Based QDI Asynchronous Circuits Based on Transition Counting

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Abstract

This paper introduces an innovative high-level method to estimate energy consumption of a well known family of asynchronous circuits at CSP level, therefore removing the need for performing time consuming SPICE simulation. Our method is based on transition count and helps the PCHB/PCFB template based QDI asynchronous circuit designers to have an early estimation of power with the accuracy of more than 80%. This estimation, obtained from commercial functional simulators, may lead to power optimization of the circuit in high levels of design.

Keywords: Energy estimation, Asynchronous, QDI, Transition Count.

1. Introduction

By introducing the portable battery-powered devices and high-speed integrated circuits, power consumption has become a critical problem in recent years. Also the cost of packaging and cooling makes this issue more challenging. Therefore, the designers are forced to consider the power consumption as an important constraint in early stages of design. Since in common methods the power consumption of a circuit is not evaluated till the final stages of circuit design flow, there is an increasing trend to estimate the power or energy consumption of circuits at earlier stages of design. In section 2 we overview some methods of power estimation in synchronous circuits.

In this paper, our focus is to introduce a method for high level estimation of energy consumption in a well-known family of QDI (Quasi Delay Insensitive) asynchronous circuits, which are based on PCHB/PCFB (Pre-Charge logic Full/Half Buffer) templates. So, at first we give a brief introduction to QDI circuits and these templates in section 3.

In order to verify the correctness of our method, we should apply it to some real circuits and compare them to results of an analog simulator with real parameters extracted from the final layout. But analog simulation of large circuits is very time consuming and may reach several days or even weeks. Section 4 is dedicated to characteristics of PCHB/PCFB energy consumption. In addition, this section introduces a method for rapid energy estimation in switch level. Using this method, we do not need to use analog simulators such as Spice and the simulation time will decrease dramatically.

Based on the results of section 4, section 5 proposes a method for estimating energy consumption of template-based asynchronous circuits in CSP level using commercial Verilog simulators.

2. Power Estimation Methods

Average power consumption of a CMOS-logic can be formulated as: $P_{avg} \approx A \times D$. Where A is the area of circuit (an estimation of circuit capacitance) and D is the average transition density of circuit.

There is more information about implementation details at lower levels such as gate and circuit levels. So, power can be estimated very accurately, but power estimation at these levels is more time-consuming. Power Simulation is a straightforward method for power estimation at these levels [1]. Due to pattern-dependency nature of power consumption to input signals, a huge number of input patterns are required for an accurate estimation. Also spatial and temporal dependencies between input signals should be considered, which is hard and time-consuming. Therefore other methods such as probabilistic and statistic methods have been proposed, in which fewer input vectors are applied for power analysis. Using these methods accuracy is somewhat scarified, in order to save time.

At higher levels such as RTL and Behavioral levels only functional or structural information about the final circuit is accessible[2][3]. But At these levels of design one can apply more power optimization approaches [2]. So power estimation at higher levels can help us to make good decisions about what to do for saving power. At these levels a relative accuracy is enough. High level power estimation techniques can be classified into these categories: Analytical techniques, Characterization-based Macro-Modeling and Fast-Synthesis based estimation [4].

Analytical power modeling techniques attempt to correlate power consumption to measures of design complexity, using very little information from the functional specification. An important class of Analytical techniques, called information-theoretic approaches, estimate average activity and capacitance factors for logic blocks based on entropy of their input and output signals.

In **characterization-based macro-modeling**, the idea is to obtain and characterize a lower-level implementation of various RTL macro blocks. Typically, a gate-level or transistor-level tool is used to estimate the power consumption of each macro block under various "training" input sequences. Based on this data, a macro-model or "black-box" model is constructed, which describes the power consumption of the block as a function of relevant parameters, *e.g.*, the signal statistics of its inputs and outputs.

Fast synthesis refers to the process of performing a limited synthesis of the RTL description that is much faster than the

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actual logic synthesis and technology mapping process. The design is mapped to a "meta-library" that typically consists of a small number of primitive cells (much smaller than a complete standard cell library). The resulting net-list is used for power estimation through gate-level simulation or probabilistic techniques.

Each of high-level power estimation methods has some drawbacks. Analytical methods have low accuracy. Also may have too much computations [3]. Characterization-base macro-modeling techniques have good accuracy, but because of characterization phase, they have too much overhead. They need a lot of memory space for storing power values. Also they need to extract macro-model parameters by analyzing the input patterns [5]. Fast synthesis-based techniques are not sufficiently accurate, because they don't consider optimization at lower levels.

These power estimation techniques are only proposed for synchronous circuits. In the published work on QDI asynchronous circuits power estimation [6], the authors proposed a simulation-based method for energy estimation. They have used a simulator called *esim* that operates on a production rule set description of a circuit. This simulator estimates the dynamic energy consumption of a QDI circuit.

In comparison with the above methods our proposed method has more benefits. It has no computation complexity. It doesn't need much memory. Its characterization overhead is negligible. It is very fast and can be evaluated with existing HDL simulation tools. Our method also has an acceptable accuracy with respect to the level it is applied to.

3. QDI Asynchronous Circuits

Among the various methods of asynchronous design [7][8][9], the method introduced by Caltech Research Group [10] is capable of having better performance, lower power consumption and being more adaptive against environment variations. This method is based on QDI timing model.

Due to the manual design difficulties in this method and the lack of automatic CAD tools, there is an increasing trend to use predefined templates [9][11].

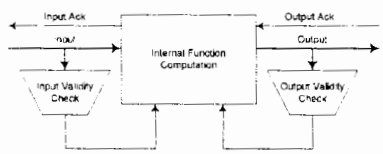

Figure 1: Structure of PCFB/PCHB Templates

At present, most QDI circuits are designed using PCHB and PCFB templates [11]. Figure 1 shows the overall structure of these templates.

Detailed structure of a PCHB template is shown in Figure 2. The template performs 4-phase handshakes [10] on both input and output channels. Input and outputs are dual-rail, so the circuit can easily determine the validity of the input or output value.

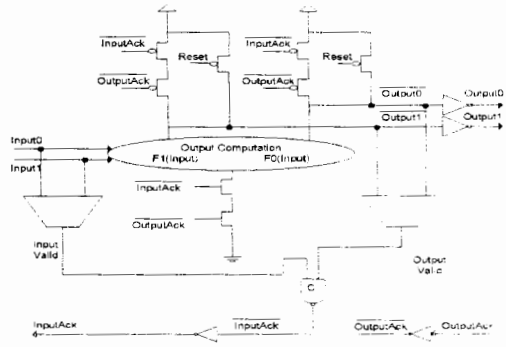

Figure 2: PCHB block diagram

As it can be seen in the figure, the output is generated after validation of input, and subsequent to validation of output, *InputAck* signal is activated. The output value is neutralized upon receiving the *OutputAck* signal, and the *InputAck* returns to zero after neutralization of inputs. Therefore, in all ports a four-phase handshake takes place. The PCFB/PCHB circuits could communicate to each other. In other words, output of any circuit could be connected to any input port of any other blocks and there is no need for any extra signal lines such as clock line. Each block is activated upon receiving a valid input. Input validity detection circuitry is similar to Figure 3.

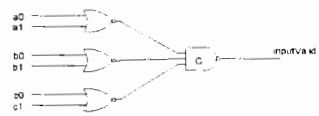

Figure 3: Validity checker circuit for a 3-bit dual-rail input

The only difference between PCFB and PCHB templates is that in the PCFB, neutralization of the output and falling of *InputAck* could happen together and independent of each other. On the other hand, in PCHB blocks *InputAck* always goes down after neutralization of the output.

Circuit of Figure 2 has normal (Unconditional) input outputs and performs simple computations on the data. PCFB and PCHB templates can perform more complicated operations such as conditional input and output actions and also can contain internal state variables [8].

3.1. Power Characteristics of QDI Circuits

QDI circuits have interesting characteristics in power consumption. First, they are inherently energy-efficient because of absence of global clock, locality of activity, automatic shut-off of inactive parts, and absence of spurious transitions (glitches) [6]. Second, Dual Rail data encoding reduces data-dependent variation in switching activity, hence making the energy estimation more accurate. Energy consumption due to glitches is null, so there is no need for using timing model. During an operation each node in the circuit has two transitions, charging and discharging transitions, and at the end of each cycle the circuit returns to its initial state. So there is no temporal dependency in these circuits. About spatial dependency, it depends on transistor sizes of each data rail.

4. Analysis of energy consumption in PCFB/PCHB Templates

The power consumed in CMOS digital circuits, in the order of importance, consists of three main parts: *Dynamic* power, *Short Circuit* power and *Static* power. Approximately 90% of power is consumed as dynamic and short circuit currents, so neglecting the static power we can say that the power consumption of a circuit with no activity is almost zero. In other words, the circuit consumes power whenever transitions occur.

According to the method proposed in [7], in order to estimate energy consumption of the circuit, we can count the number of transitions on the outputs. Using this method, there is no need to use analog simulators such as SPICE and the simulation time will decrease dramatically. In circuits with monotonous and regular fan-out like data-paths, energy consumption can be estimated by counting the transitions on the gate outputs, with an accuracy of more than 90%. But in case of control logic, which has a random nature, the accuracy falls below 60% [7], because the fan-out does not contribute to transition counting in this method.

To solve the fan-out problem we propose to count the transitions on the input of gates. Using this method, a transition on the output of a gate connected to three gates is counted three times, so fan-out is considered automatically.

To increase the precision of our estimations, we should have the description of the circuit at lower levels. We propose to use this method for circuits described in switch level. We have used **pmos** and **nmos** transistor models of Verilog HDL for this purpose.

Using the method introduced above we can estimate the transition count and therefore energy consumption of individual parts of a PCFB/PCHB template as building block of QDI asynchronous circuits. Table 1 shows the number of transitions and the transistor count of three main parts of a 4-bit PCFB buffer. The transitions are counted by applying random inputs.

Table 1: Number of transistors and transitions in three main parts of a 4-bit PCHB buffer.

	Internal Circuit	Output Validity	Input Validity	Total
Transistors	110	38	36	184
%	59.7%	20.6%	19.5%	
Transitions	101	32	22	155
%	65.1%	20.6%	14.1%	

Table 1 shows that almost 35% of total transitions have occurred in I/O-validity-check circuits. This value increases proportionally to the number of input and output lines.

As another example, Table 2 depicted the details of a 4-bit Galois Field Adder implemented in PCHB with two 4-bit inputs and a 4-bit output.

Comparing the results of Table 1 and Table 2, we can conclude that the power consumption of input-validity circuit in GF Adder is about twice as that of similar portion in 4-bit Buffer. This is due to doubling the number of input bits of GF adder. In another word, transitions of input and output validity circuitry are proportional to number of bits.

Table 2: Number of transistors and transitions in three main portions of a 4-bit PCHB Galois Field Adder for random inputs.

	Internal Circuit	Output Validity	Input Validity	Total
Transistors	118	38	72	228
%	51.7%	16.6%	31.5%	
Transitions	140	32	56	228
%	61.4%	14%	24.5%	

In a design, synthesized based on PCHB and PCFB template buffers, most of the elements are regular such as *InputValid* and *OutputValid* and their activity is linear according to input and output width. But the internal part of the buffers including the output function is irregular.

Transitions of different parts of a simple 1-bit PCHB-PCFB buffer and the relation between a 1-bit and n-bit buffer are required to estimate the transitions of an x-bit buffer, in a simple transfer of input to output. This relation is evaluated according to the transitions of 1-bit to 32-bit buffers. Table 3, containing transitions of 1-bit to 8-bit buffers, is used for this purpose.

Table 3: Transition counts of main parts of PCHB buffers

Buffer length	1	2	3	4	5	6	7	8
Input Valid	4	14	18	22	26	30	34	56
Output Valid	8	20	27	32	38	42	46	72
Internal Circuit	44	63	82	101	120	139	158	177

The relation between the transition count and buffer size as shown in Figure 4, is almost a linear relation and can be modeled as y=ax+b.

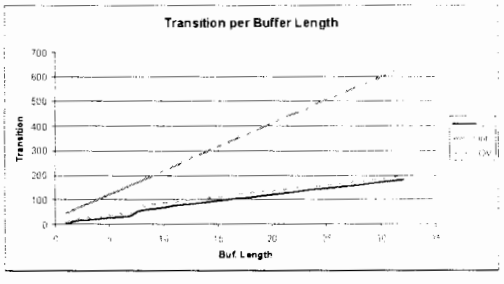

Figure 4: Linear relation between buffer size and transition count

The internal part of the templates as shown in figure 2 has a common part in all templates plus a function to evaluate each rail of the output. This function is different in each template of different functionality. The simplest form of a function is just a transistor used in simple buffers. As a practical circuit, consider a *GF Constant Multiplier* with the complex function shown bellow.

$$Z = \alpha^9 A \begin{cases} z_0 = a_1 \oplus a_3 \\ z_1 = a_0 \oplus a_1 \oplus a_2 \oplus a_3 \\ z_2 = a_1 \oplus a_2 \oplus a_3 \\ z_3 = a_0 \oplus a_2 \oplus a_3 \end{cases}$$

As shown in Table 4 if we estimate the internal part of the 4-bit GF multiplier with its equivalent 4-bit buffer, there is an inaccuracy of about 5.1%. This is a complex function and for

the common functions, that are simpler, there is a better accuracy in estimation. Therefore, we can estimate the transition count of each template considering the length of input and output channels. The accuracy of this estimation is almost 95%, in this example, regardless of function type.

Table 4: Number of transistors and transitions in three main parts of a 4-bit PCHB GF Constant Multiplier.

	Internal Circuit	Output Validity	Input Validity	Total
Transistors	126	38	36	200
%	63%	19%	18%	
Transitions	109	32	22	163
%	66.8%	19.6%	13.4%	

5. Transition Counting in CSP Level

QDI circuits are modeled at the behavioral level using a CSP [10] derived language. Then the initial design is decomposed to smaller CSP blocks and this procedure is continued to get the simple elements. The elements generated by this method are modeled as processes communicating to each other using input and output channels. Communications between different processes are via handshaking and in most cases include data transfer as well. This can be viewed as read or write operations. The following code describes a template performing logical AND.

READ(A, TmpA)
READ(B, TmpB)
TmpOut = TmpA AND TmpB;
WRITE(Out, TmpOut)

In our method the codes are written in Verilog and the handshakes are modeled with PLI "Read" and "Write" macros [12]. Modifying these macros, transitions on the input and output of a PCHB/PCFB buffer are calculated automatically as sum of the transitions of *InputValid*, and *OutputValid* of each buffer based on the 1-bit buffer and the related linear equation. The Internal transitions are also estimated as a simple buffer with equal length.

6. Experimental Results

Applying this method to some parts of a Reed-Solomon decoder shows that the results in Table 5 have an inaccuracy of more than 15%.

Table 5: Experimental results

Circuit	Transition count at transistor-level	Transition count at CSP	Error
Chien	12343	10708	0.13
Error Corrector w. error	3206	2854	0.10
Error Corrector wb.error	2524	2476	0.02
Syndrome	15539	13760	0.11

This percentage of inaccuracy is acceptable since the estimation is in high level.

7. Conclusion

This paper has introduced a new method for energy estimation of template-based QDI circuits based on transition count at two different levels of abstraction, transistor-level (+95% accuracy), and CSP-level (+80% accuracy) based on the transistor-level results. Experimental results compared to the results from SPICE shows that our method estimates energy with an accuracy of more than 80% at a high level of abstraction. This estimation at this level helps the designers to have an early power optimization with no need to time consuming asynchronous circuit synthesis, and slow transistor-level energy estimation tools. This accuracy is highly acceptable, for it is in the high level and estimation is made without any extra work of designer, and it is estimated in simulation phase.

References

[1] Farid N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits", IEEE Transactions on VLSI Systems. VOL. 2, NO. 14, December 1994.

[2] P. Landman, "High-level power estimaton," in Proc. Int. Symp. Low Power Electronics & Design, pp. 29–35, Aug. 1996.

[3] E. Macii, M. Pedram, and F. Somenzi, "High-Level Power Modeling, Estimation, and Optimization", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, VOL. 17, NO. 11, November 1998

[4] S.Ravi , A.Raghunathan and S.Chakradhar . "Efficient RTL Power Estimation for Large Designs" Computer and Communication Research Labs NEC USA , 2000.

[5] Subodh Gupta and Farid N. Najm, "Power Macromodeling for High Level Power Estimation", ACM DAC 1997.

[6] Paul I. Penzes and Alain J.Martin, "An Energy Estimation Method for Asynchronous Circuits with Application to an Asynchronous Microprocessor", Caltech 2002.

[7] D. J. Pursley, S. L. Coumeri, D. E. Thomas, "The Effectiveness of Transition Counting as a Predictor of Relative Energy Consumption", *Technical Report*, CMUCAD97-43, Department of ECE, CMU, 1997

[8] A.M. Lines, Pipelined Asynchronous Circuits. *M.Sc. Thesis, California Institute of Technology*, June 1995, revised 1998.

[9] K. Saleh, H. Pedram, et. al. "Synthesis Tool for Asynchronous Circuits Based on PCFB and PCHB", *Proc. of CSICC2004*, February 2004.

[10] Alain J. Martin, "Synthesis of Asynchronous VLSI Circuits",*Caltech, CS-TR-93-28*, 1991.

[11] A. J. Martim, M. Nystrom, et. al. "The Lutonium: A Sub-Nanojoule Asynchronous 8051 Microcontroller", *Proceedings of the Ninth International Symposium on Asynchronous Circuits and Systems (ASYNC'03)*, 2003

[12] A. Seifhashemi, H. Pedram, "Verilog HDL, Powered by PLI: a Suitable Framework for Describing and Modeling Asynchronous Circuits at All Levels of Abstraction", *Proc. Of 40th DAC, Anneheim, CA, USA*, June 2003